

PAGE 2/9 \* RCVD AT 4/10/2006 5:03:01 PM [Eastern Daylight Time] \* SVR:USPTO-EFXRF-2/14 \* DNIS:2738300 \* CSID:5129966854 \* DURATION (mm-ss):20-52

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9

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Date: April 10, 2006  
To: Richard A. Booth – 2812  
Location: United States Patent and Trademark Office  
Fax No.: (571) 273-8300  
From: Kim-Marie Vo - 50,714  
Subject: 10/811,461 – Marius K. Orlowski, et al. - SC13240TP

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## MESSAGE:

Enclosed herewith, please find a FORMAL AMENDMENT for filing in the below-identified application.

## ALL ITEMS MARKED WITH AN "X" ARE INCLUDED:

1.	x	1 page Facsimile Cover Sheet
2.	x	1 page Notice of Appeal (in duplicate)
3.	x	1 page Fee Transmittal (in duplicate)
4.	x	1 page Pre-Appeal Brief Request For Review
5.	x	3 page Pre-Appeal Brief Statement

Paid by Deposit Account: 503079, Freescale Semiconductor, Inc. \$500

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*Kim-Marie Vo*  
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## PLEASE GIVE THESE PAPERS TO:

EXAMINER: Richard A. Booth  
GROUP ART UNIT: 2812  
SERIAL NO.: 10/811,461  
FILED: MARCH 26, 2004  
Inventor: Marius K. Orlowski, et al.

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PTO/SB/33 (07-05)

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<b>PRE-APPEAL BRIEF REQUEST FOR REVIEW</b>		Docket Number (Optional) SC13240TP	
I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to "Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450" [37 CFR 1.8(a)]  on <u>April 10, 2006</u> Signature <u>Dora Hudgins</u>  Typed or printed name <u>Dora Hudgins</u>		Application Number 10/811,461	Filed March 26, 2004
		First Named Inventor Marius K. Orlowski	
		Art Unit 2812	Examiner Richard A. Booth
Applicant request review of the final rejection in the above identified application. No amendments are being filed with this request.  This request is being filed with a notice of appeal.  The review is requested for the reason(s) stated on the attached sheet(s). Note: No more than five (5) pages may be provided.  I am the <input type="checkbox"/> applicant/inventor. <input type="checkbox"/> assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96) <input checked="" type="checkbox"/> attorney or agent of record. Registration number <u>50,714</u>  <input type="checkbox"/> attorney or agent acting under 37 CFR 1.34 Registration number if acting under 37 CFR 1.34 _____  NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.			
<div style="text-align: right; margin-right: 100px;">           Signature  <u>Kim-Marie Vo</u>          Typed or printed name  <u>(512) 996-6839</u>          Telephone number       </div>			
<input checked="" type="checkbox"/> *Total of <u>1</u> forms are submitted			

The collection of information is required by 35 U.S.C. 132. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality if governed by 35 U.S.C. 122 and 37 CFR 1.11, 1.14 and 41.6. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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SC13240TP

UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT(S) Marius K. Orlowski, et al. GROUP ART UNIT: 2812  
APPLN. NO.: 10/811,461 EXAMINER: Richard A. Booth  
FILED: March 26, 2004  
TITLE: METHOD FOR FORMING A SEMICONDUCTOR DEVICE HAVING A  
NOTCHED CONTROL ELECTRODE AND STRUCTURE THEREOF

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on April 10, 2006

Dora Y. Huggins  
Signature

Dora Huggins  
Printed Name of Person Signing Certificate

**PRE-APPEAL BRIEF STATEMENT**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

Responsive to the Office Action dated March 31, 2006, and Examiner's comments with regard thereto, please enter the following Pre-Appeal Brief Statement in the above-entitled application, without prejudice or disclaimer.

If Applicant has overlooked any additional fees, or if any overpayment has been made, the Commissioner is hereby authorized to credit or debit Deposit Account 503079, Freescale Semiconductor, Inc.

SC13240TP

REMARKS

Claims 16-30 are pending and are under final rejection. There are two issues over which Applicants and the Examiner disagree. Applicants will address the Examiner's response to these issues below.

First Issue

Applicants submit Mansoori fails to teach or suggest "forming a first patterned conductive layer...", "forming a second patterned conductive layer...", and "selectively removing portions of the first and second patterned conductive layers..." because Mansoori patterns or selective removes portions of elements 1610 and 1620 but does not do both. (More details as to this argument are provided in Applicants' previous response.)

The Examiner contends, "...the limitation is shown since a single process step can be broken up into an infinite number of smaller process steps and therefore this process step can be represented by an intermediate figure between figures 19 and 20." Thus, the Examiner submits that although Mansoori's text and figures fail to teach or suggest all features of Applicants' claims, because Mansoori teaches process steps one can, without teaching or motivation from Mansoori or another reference, infer that Mansoori teaches or suggests other process steps that Mansoori is silent as to. Applicants fail to see where this is cited in the MPEP or where this has become law.

Instead, the MPEP and the law go against the Examiner's position. The Examiner's position improperly reads limitations out of the claims. More specifically, the Examiner's is reading the phrase "patterned" out of the phrases "first patterned conductive layer" and "second patterned conductive layer" or alternatively, is ignoring the phrase "selectively removing portions of the first and second patterned conductive layers." This is improper. MPEP 2143.03 addressed this issue and states,

To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). "All words in a claim must be considered in judging the patentability of that claim against the prior art." *In re Wilson*, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970).

SC13240TP

Second Issue

Applicants submit Mansoori also fails to teach or suggest, "wherein after selectively removing portions of the first and second patterned conductive layers, the first and second patterned conductive layers have lengths that are substantially equal." The Examiner and Applicants agree that in the cross-sections shown elements 1610 and 1620 do not have substantially equal lengths. However, the Examiner contends that elements 1610 and 1620 do have substantially equal lengths in the dimension into the page. Applicants fail to see where Mansoori teaches or suggests this. In contrast, Mansoori teaches that the "layer 1610 will etch faster than the other layers due to an enhanced sensitivity to an etchant." (See paragraph [0056].) Therefore, layer 1610 will not have the same dimensions as other layers, such as layer 1620. Furthermore, Mansoori fails to teach or suggest that the dimension into the page is not etched for the layers 1610 and 1620. Therefore, Mansoori fails to teach that layers 1610 and 1620 have lengths that are substantially equal.

Please contact Applicant's practitioner listed below if there are any issues that can be resolved by telephone.

Respectfully submitted,

SEND CORRESPONDENCE TO:

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By: 

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